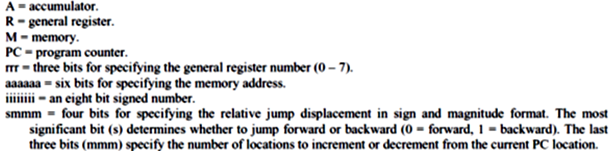
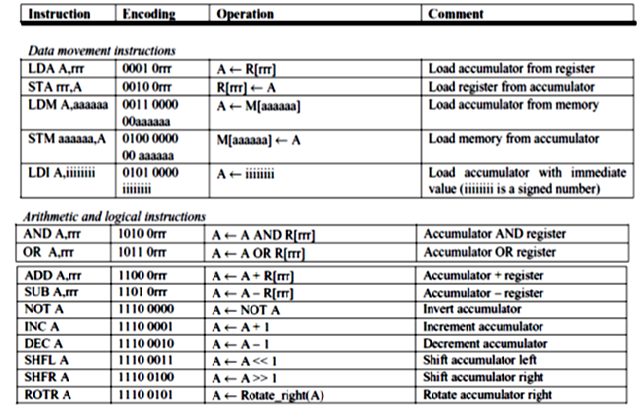
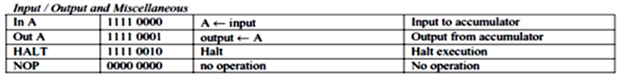
Course Project: Due: May 2nd.

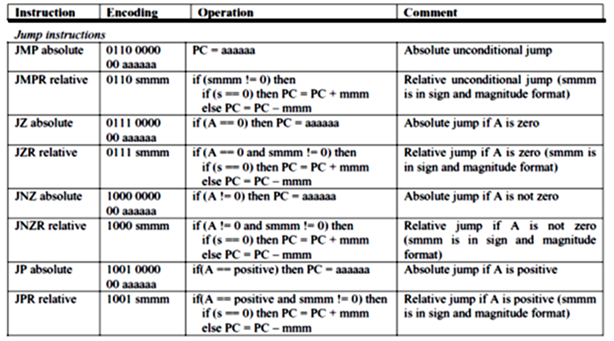
The Instruction Set of a simple CPU (lets name it my\_CPU) is described in Table 1 , where

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**Table 1: Informal description of The Instruction set of a simple CPU**





The datapath is provided in Fig.2. It is modified from the original version due to multiple problems: MA is added. Immediate value (imm) is provided directly from the Memory to Accumulator. Number of cycles per instruction: from 2 to 4(see, Modified DP notes)

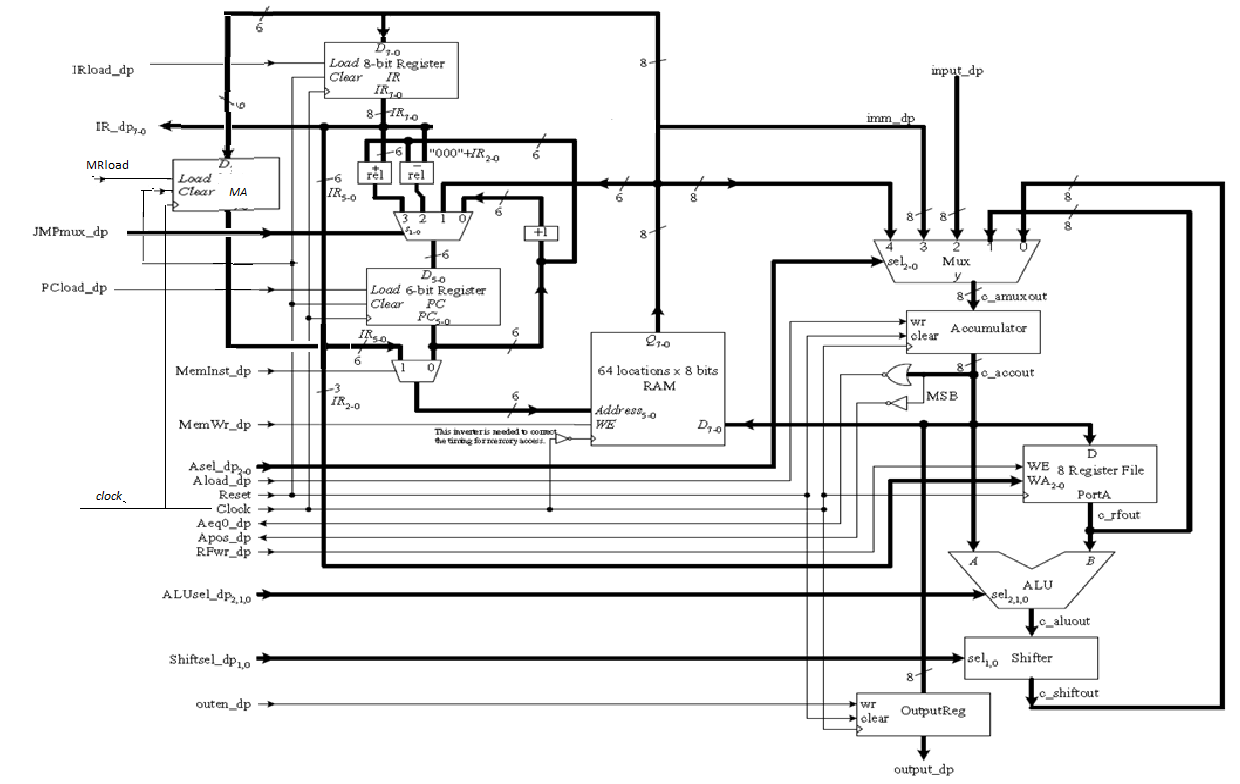


Fig.2 Data path of my\_CPU

Assignment:

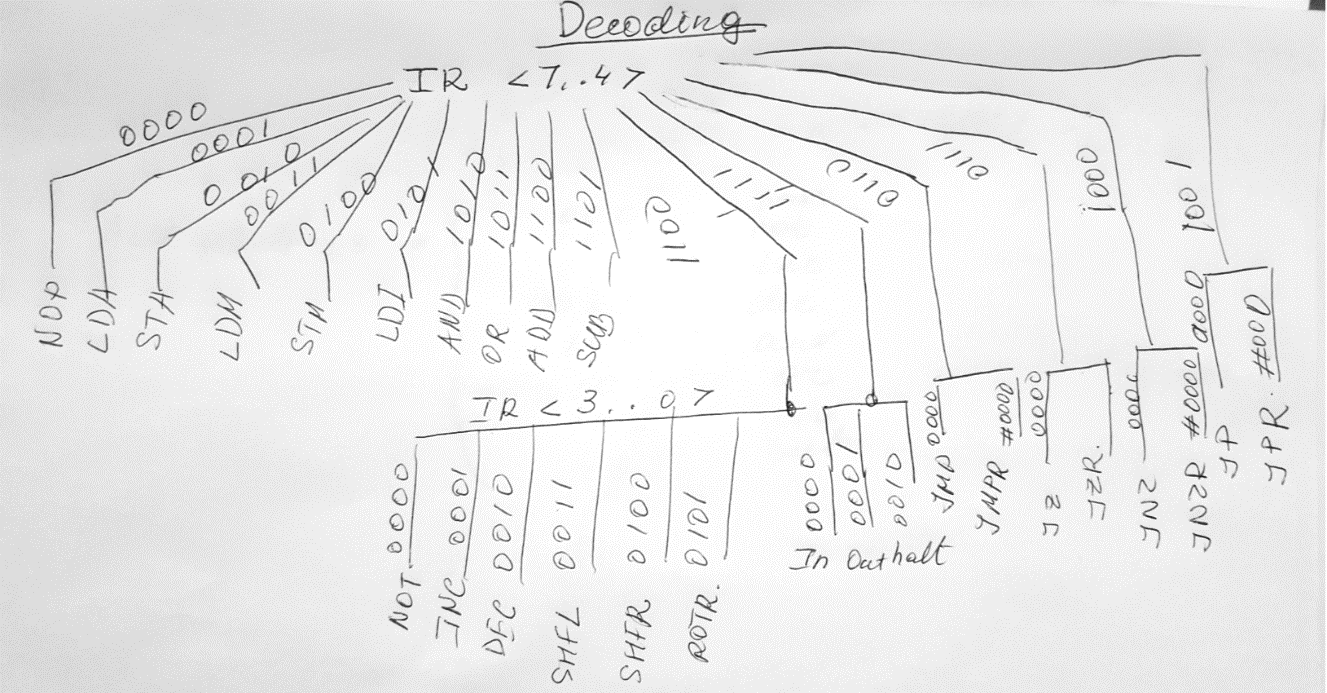
1. Write Verilog modules for the complete design, including the control Unit.
2. Write a test code to include all instructions and design a testbench.
3. Provide the simulation results

Grading:

1. Design of the control unit (paper design : schematic)- 10 points
2. Verilog codes for all modules tested with waveforms-30 points
3. All above + testbench design +snapshots of ModelSim simulation-45 points

Notes on the datapath and control

1. Many instructions of length of 1 byte, some of 2 bytes: these instructions are: LDM, STM, JNZ, LDI, JZ, JP
2. PC is incremented by 1, and if the opcode indicates that instruction needs the second byte, the latter will be fetched anyway. Decoding of instructions: two levels: first level is based on IR<7..4>, and the second level reads IR<3..0>. See below



1. ALUsel\_dp 2,1,0 bits and shift\_dp as for the General Datapath :

